Electrical Yield and Reliability Issues of Ultra High Density Interposers and Update on Advanced Integration Program at BRIDG

Dr. John Allgair

Dr. Amit Kumar

BRIDG is a not-for-profit, industry-friendly public-private partnership for the manufacturing of advanced smart sensors and imagers - formerly known as

iCAMR

Overview

NEOCITY and BRIDG overview

- Fab site and facility
- Equipment
- Roadmap

Advanced System Integration Program

- Ultra High Density Interposer Project

Next Steps

The Goal… NEOCITY

Purpose:

Our purpose is to create a more financially sound and diverse economy in Central Florida by serving as a catalyst for creating high wage job opportunities for residents and the broader Southeast region of the United States.

Our infrastructure is built to create this economy based around a highly versatile nanoscale microelectronics manufacturing and development center. We build and execute technology-specific roadmaps that align to our capital and operational expectations.

As a not-for-profit, public-private partnership, and as good stewards of our region's investment, our single largest metric of success is the creation of jobs in the region.

BRIDG – A New 200mm Wafer Fab in Florida

109,000 sq ft facility
- 26,500 sq ft, Class-100 CR
- 9,400 sq ft, Class-10K CR
- 10,000 sq ft, Lab Space

"Trust-Enabled", ITAR

Nano-Electronics Fabrication Facility: Cleanrooms and Labs

Public Private Partnerships

Infrastructure to Drive Concepts to Commercialization

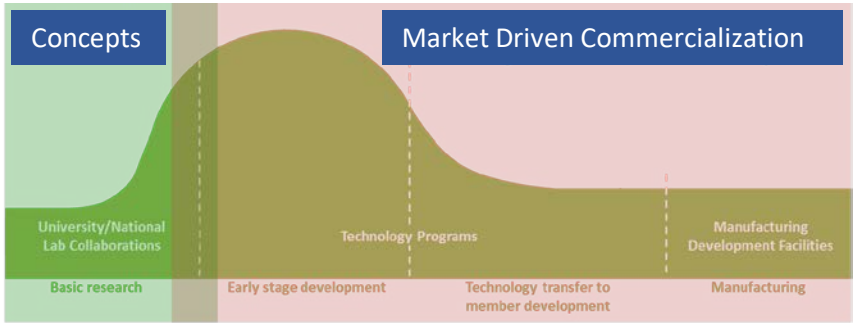
University/Lab Research

CONCEPT:

- Creative ideas
- Centers of Excellence
- Novel techniques & innovative technologies
- Fundamental research
- Market Intelligence

BRIDG INFRASTRUCTURE:

- Accelerate high potential technologies into next generation products & systems
- BRIDG and partners develop and provide commercialization infrastructure
- Capability for proof of concept, custom development, pilot production
- IP Protection, Funding Coordination
- Small Business Enablement

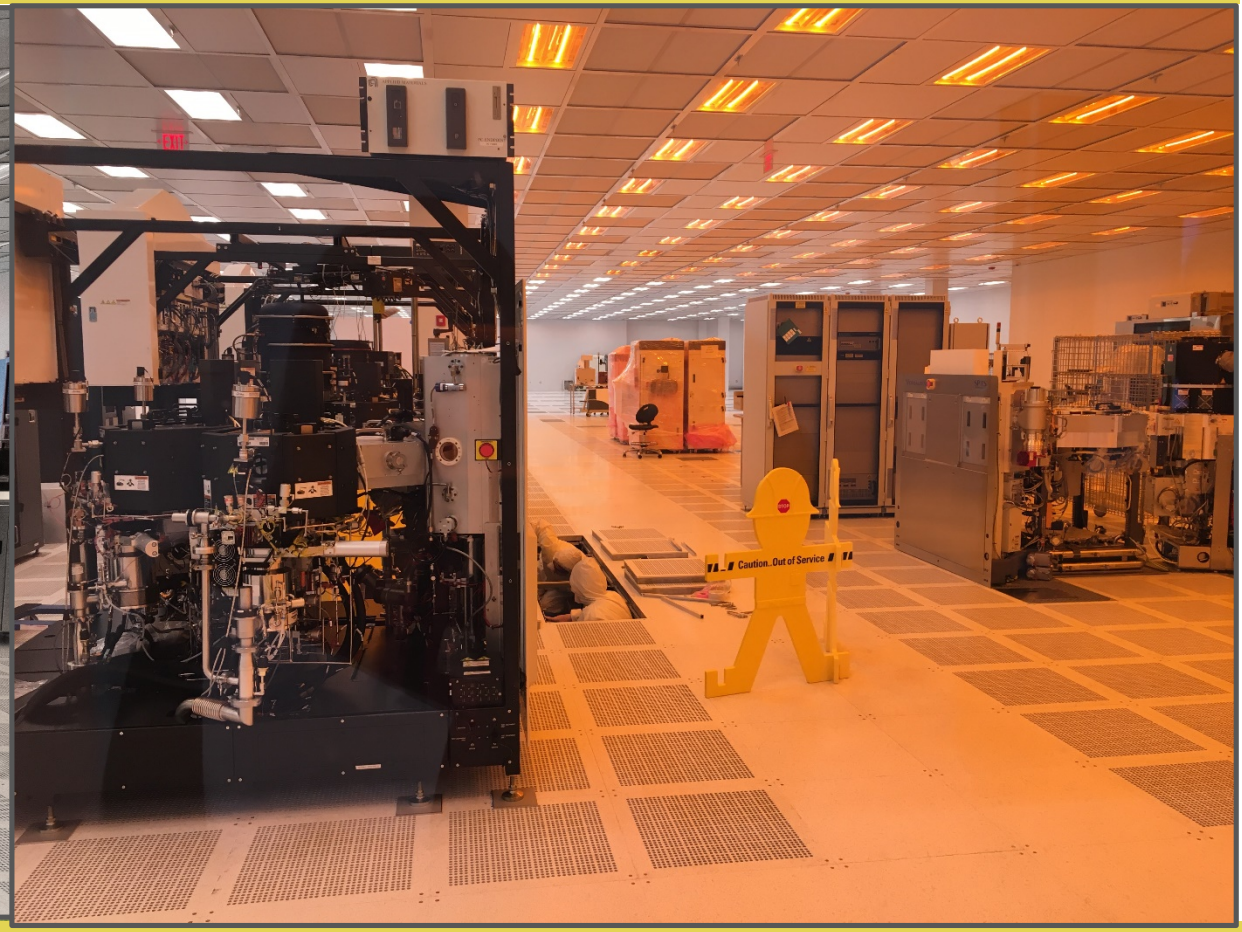


Volume Manufacturing

COMMERCIALIZATION:

- Advanced Imagers, Sensors and Photonics
- Heterogeneous System Integration
- Advanced Materials for RF, Power and Sensing Applications
- Emerging technologies, including ReRAM and direct patterning
- Hardware based cybersecurity

Core Tool Installations Complete June 2018



200mm Tool Installation and Calibration

Equipment Overview

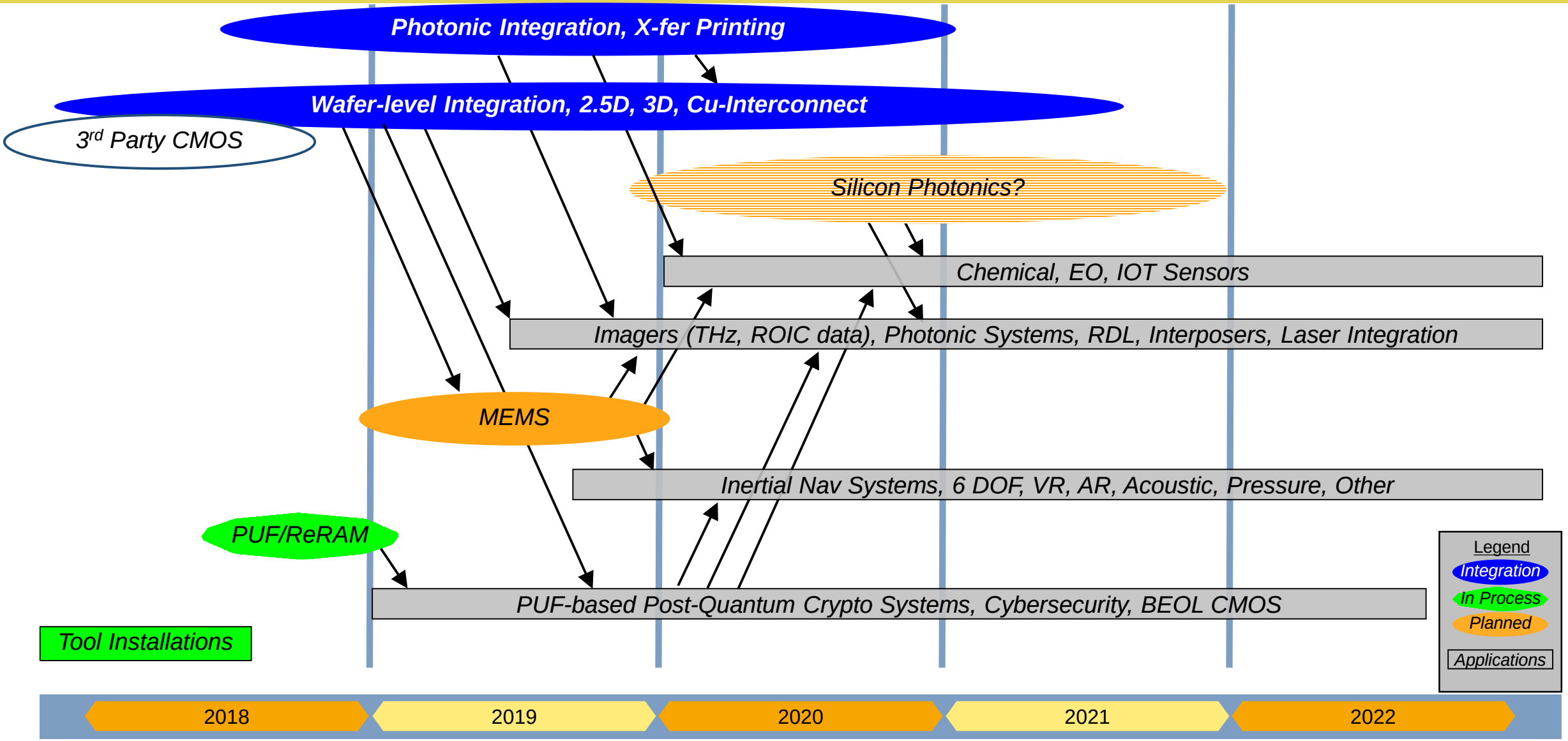
Equipment Acquisitions

- Asher – Trion Apollo III
- Batch Solvent Tool
- Bond Aligner / Mask Aligner – SUSS MABA8 Gen4Pro
- Bond Alignment Metrology – SUSS DSM8/200 Gen2
- Bonder, Permanent – SUSS XB8
- Box Washer – Flouroware HTC-810
- CD SEM – SEM5 Hitachi 9200
- CMP – AMAT Mirra Trak (Cu)
- CMP – AMAT Mirra Trak (Oxide/W)
- Coater / Developer – TEL ACT8
- CVD HDP – AMAT Centura
- CVD – AMAT Centura (W)
- CVD – Novellus C2 Sequel (SiN, SiO2)
- Deep Silicon Etch and Wafer Dicing – SPTS Rapier
- Deep Silicon Etch and Wafer Thinning (Plasma) Tool
- Defect Inspection – KLA 2139 - Bright Field
- Ellipsometer Film Thickness, Stress Measure – KLA F5x
- Etch – AMAT CENTURA (Metal Etch)
- Etch – AMAT CENTURA (Oxide Etch)
- Etch – AMAT CENTURA (Poly Etch)
- Evaporator – Temescal UEFC-4900 (Au, Pt, Ti, Al, etc.)
- Furnaces – Tel Alpha 8s (Anneal, Oxide, Nitride, Poly, Diffusion)
- Goniometer – Rame-Hart
- Ion Implant – Varian E500 (Medium Current)
- Laser Scribe – Lumonics GSI
- Microscope
- Overlay – Inspectrology
- Photoluminence/Defect Measure – KLA Cadela CS920
- PVD – AMAT Endura (Cu, TaN, Al, TiN, RPC)
- Rapid Thermal Annealing (RTA) – Manual
- Single Wafer Wet Processing – SEMSYSCO Triton (Electroplating, Liftoff, Solvent Strip and Acid Clean)
- Stepper – Nikon i-Line i12
- Wafer Scrubber – OnTrak DSS2
- Wet Bench – JST (Acid, Base)
- Xceleprint
- XRD, XRR, XRT – Panalytical X'PERT3MRD
- 4-Point Probe – CDE
- Metal Oxide Chemical Vapor Deposition (MOCVD) Tool

Future Equipment

- AFM
- Atomic Layer Deposition (ALD) Tool
- De-Bonder
- Fine Line Lithography – 193nm / e-beam
- Hall Measurement Tool
- High Alignment Accuracy Pick and Place Tool
- Materials Coater
- Molecular Beam Epitaxy (MBE)
- Profiler
- Rapid Thermal Annealing (RTA) – Automated
- SAM
- SEM with FIB
- Tape and Frame
- Temporary Bonder
- Transmission Electron Microscope (TEM)
- Vector Network Analyzer
- Wafer Grinder

BRIDG Technology Roadmap v0.7



Overview

NEOCITY and BRIDG overview

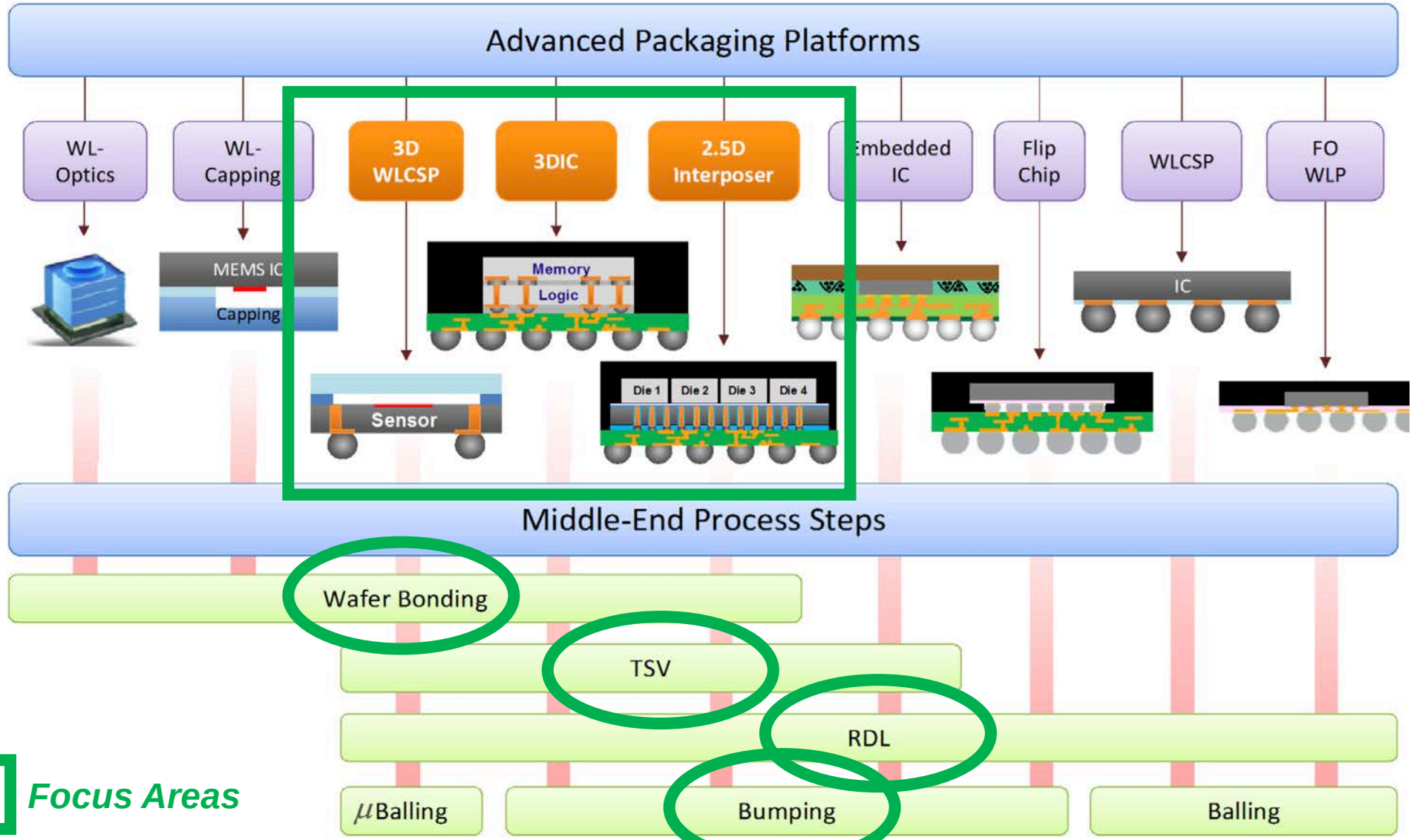
- Fab site and facility
- Equipment
- Roadmap

Advanced System Integration Program

- Ultra High Density Interposer Project

Next Steps

Advanced Packaging Industry Overview



Focus Areas

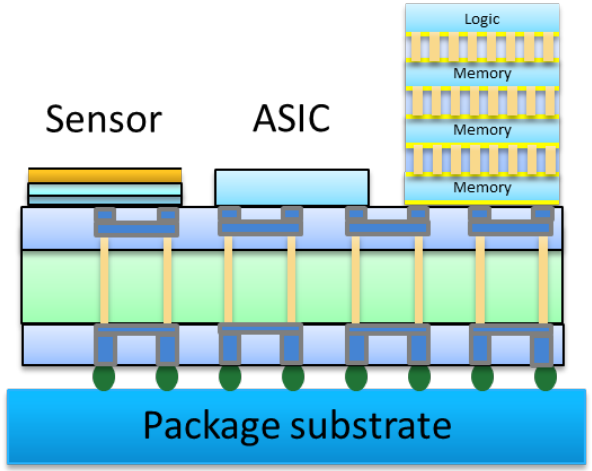
Source Yole

Advanced System Integration Program

Provide solutions for size, weight and power reduction which address challenges faced by conventional scaling

Improved performance

- Heterogeneous Integration (Si, III/V, Photonics)
- Ultra-High Density (Wide I/O - 10^6)
- Power Consumption and System Response Time
- Robust Operating Temperature Range (77K to 673K)



Improved Form Factor

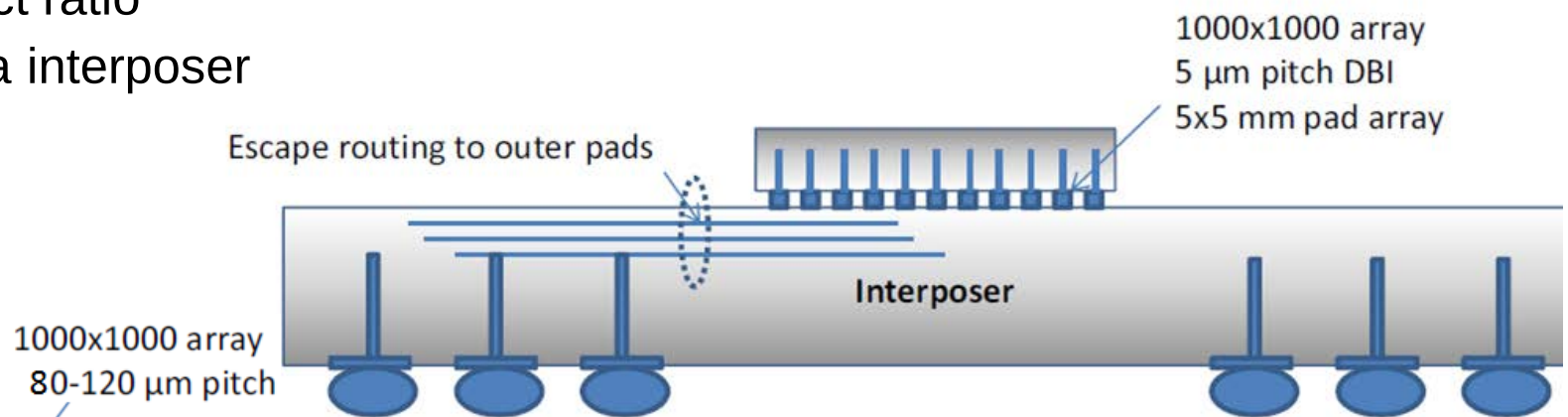
Transform traditional sensing techniques allowing continuous monitoring and the ability to monitor more…

Ultra High Density Interposer (UHDI) Project (Active since Jan 2016)

Develop fabrication and assembly process for an order of magnitude beyond current state-of-the-art 2.5D/3D Integration

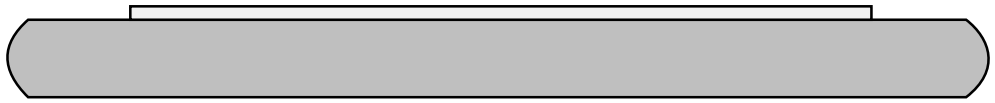
Challenges:

- Bonding yield
  - 10^6 I/O in 5×5 mm^2 area
- Wafer-to-wafer or chip-to-wafer alignment/placement accuracy
  - 0.5 μm – 1 μm post bond accuracies
- Multilayer routing capability
  - 6-13 layers to escape 10^6 I/O on a 5 μm pitch with 60 nm L/S
- Large area nm lithography
  - Interposer routing lies outside of the reticle field (80×80 mm^2 up to 120×120 mm^2)
- Through silicon via diameter and aspect ratio
- Warpage and stability of thin large area interposer

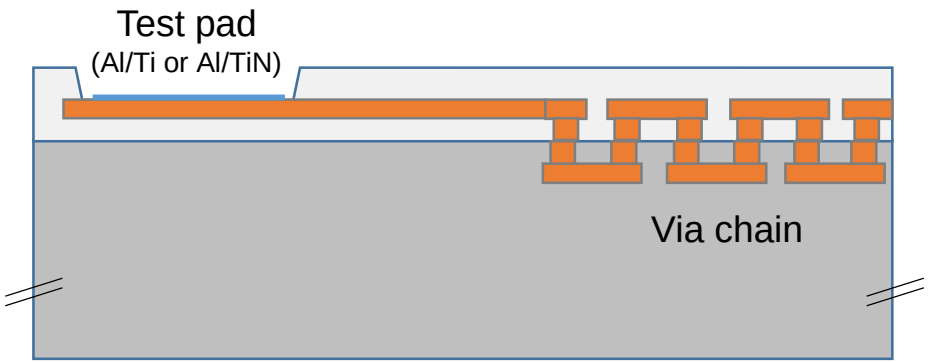


UHDI Electrical Test Vehicle – Phase 1

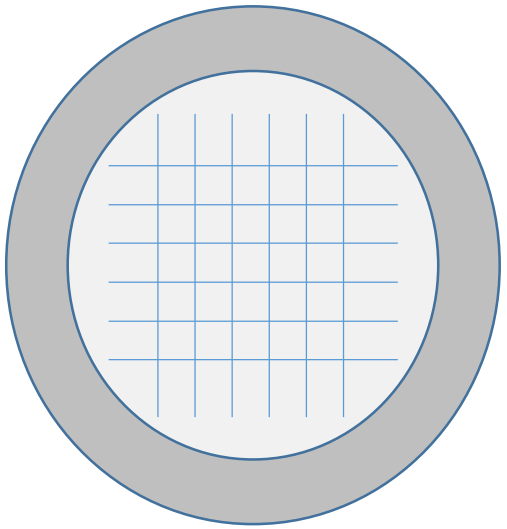
The purpose of this test vehicle is to assess the ability of the DBI process to bond 1M I/O at 5 µm or smaller pitch using a wafer-to-wafer bonding process and to obtain data on the yield and reliability of the bonding process.



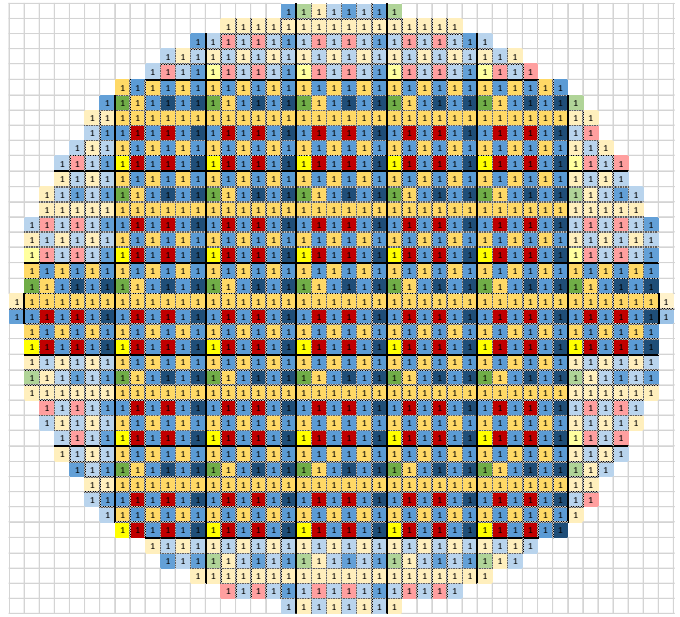
8” wafer bonded to 8” wafer, after thinning
(not to scale)



Cross section showing metal layers, vias, and test pads
(not to scale)

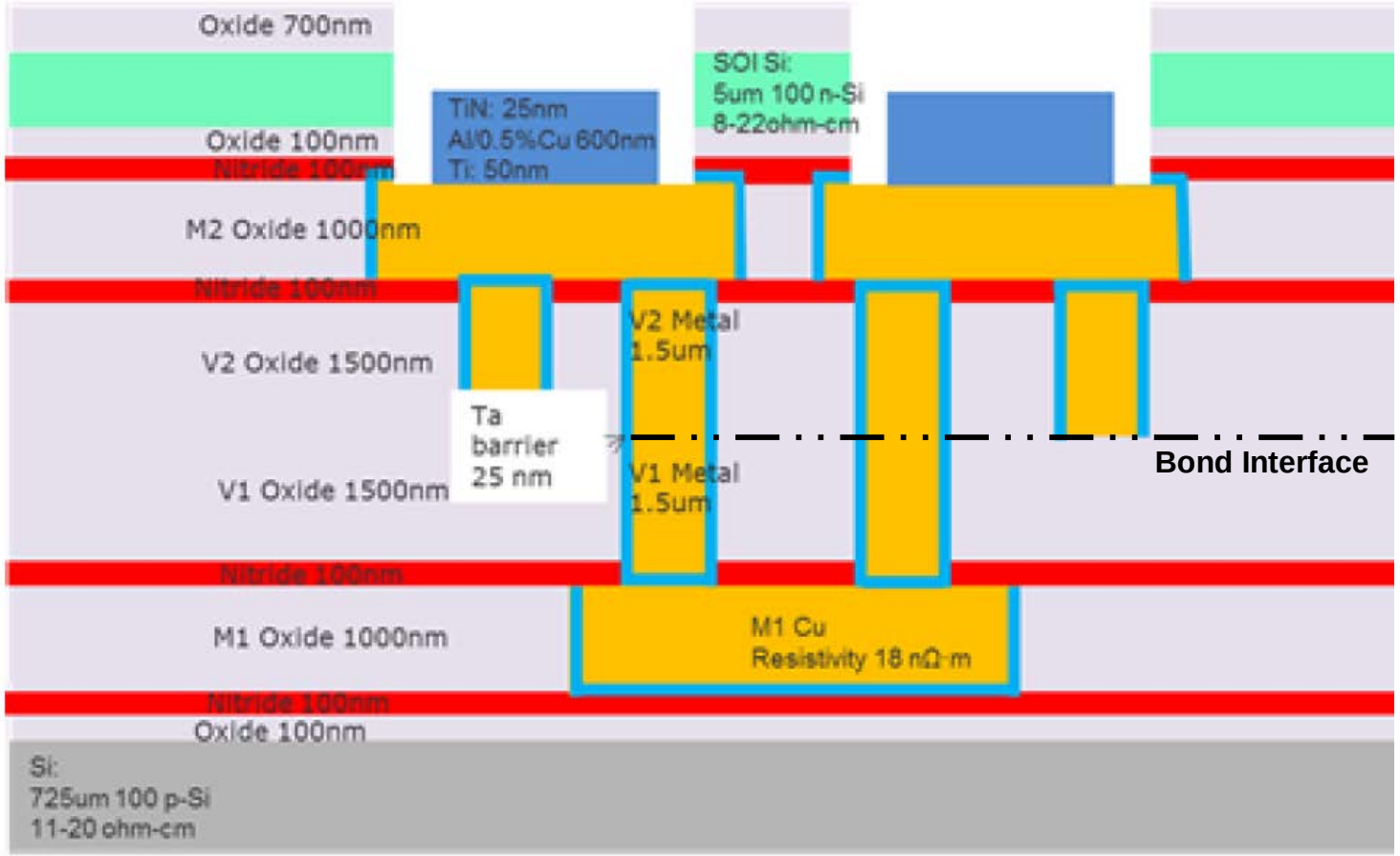


Top view showing
wafer diameters and
stepped die



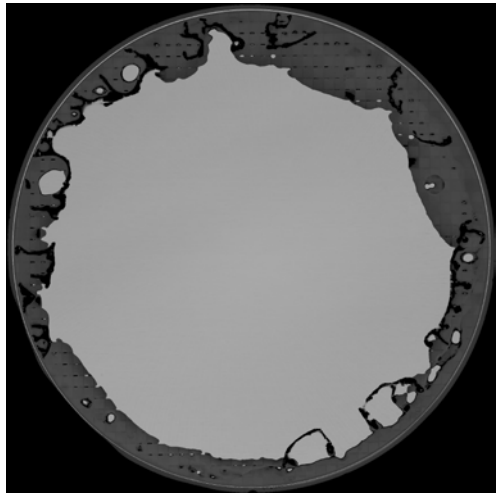
36 Cells per Die
- 13 standard 1M DBI via chains
  - taps @ 2,20,200,2k,20k,200k,1M
- 4 misaligned DBI via chains
  - -0.5, -0.25, +0.25, +0.5 µm
- 13 standard combs
- 4 misaligned combs
- 1 Serpentine Cell w/6 serpentines
  - M1/M2, 1/1.2/1.4 µm
- 1 EM Utility Cell

UHDI Electrical Test Vehicle Process Overview

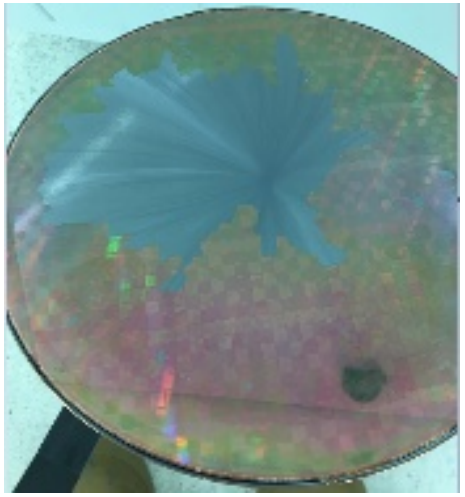


- Single damascene, copper/silicon dioxide fabrication process w/1um thickness
- EVG Gemini bonder with Direct Bond Interconnect (DBI) process
- Low Temperature Oxide (LTO) & High Temperature Oxide (HTO) splits
- Sonix CSAM void/defect metrology
- TEL P-12XL probe station w/Agilent 4073A series parametric tester

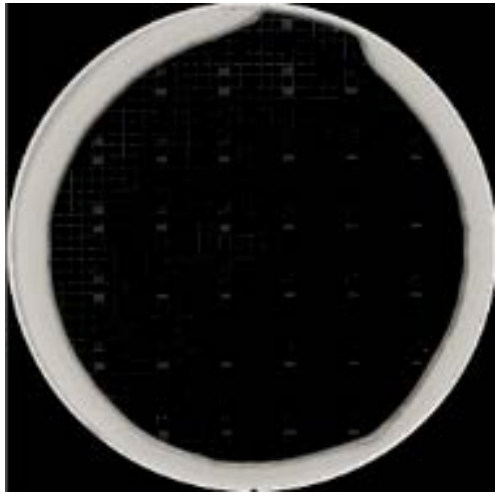
UHDI Electrical Test Vehicle LTO Results



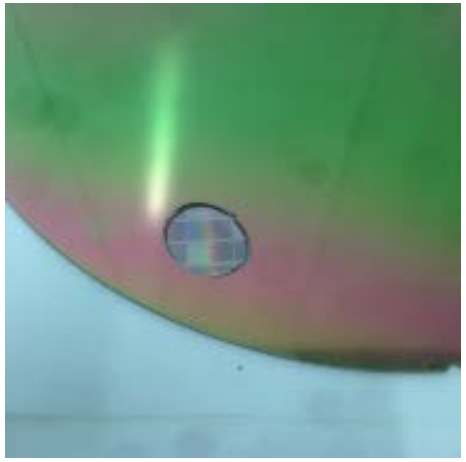
Pair 1: Si/Si, Large Void after final anneal



Pair 2: Si/Si, de-bonding at CMP prior to stop on SOI

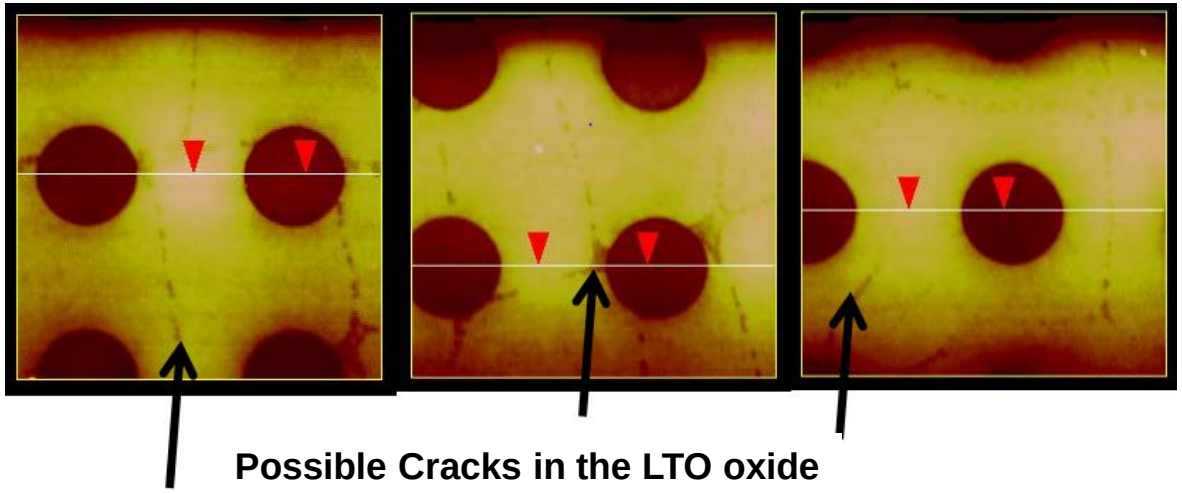


Pair 3: Si/Si, Edge de-bonding after final anneal



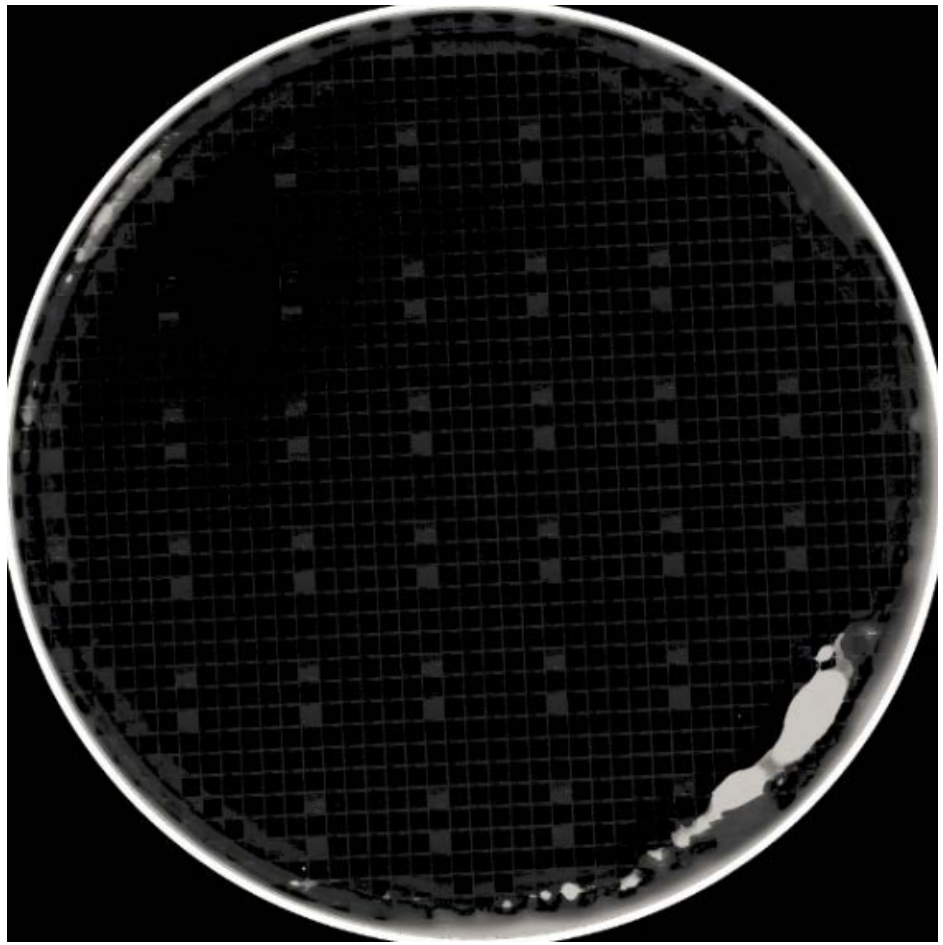
Pair 4: Si/FusedSi, pop out at CMP prior to stop on SOI

- LTO chosen to improve CTE mismatch between Si and FusedSi
- Bonding attempts for LTO oxide were unsuccessful

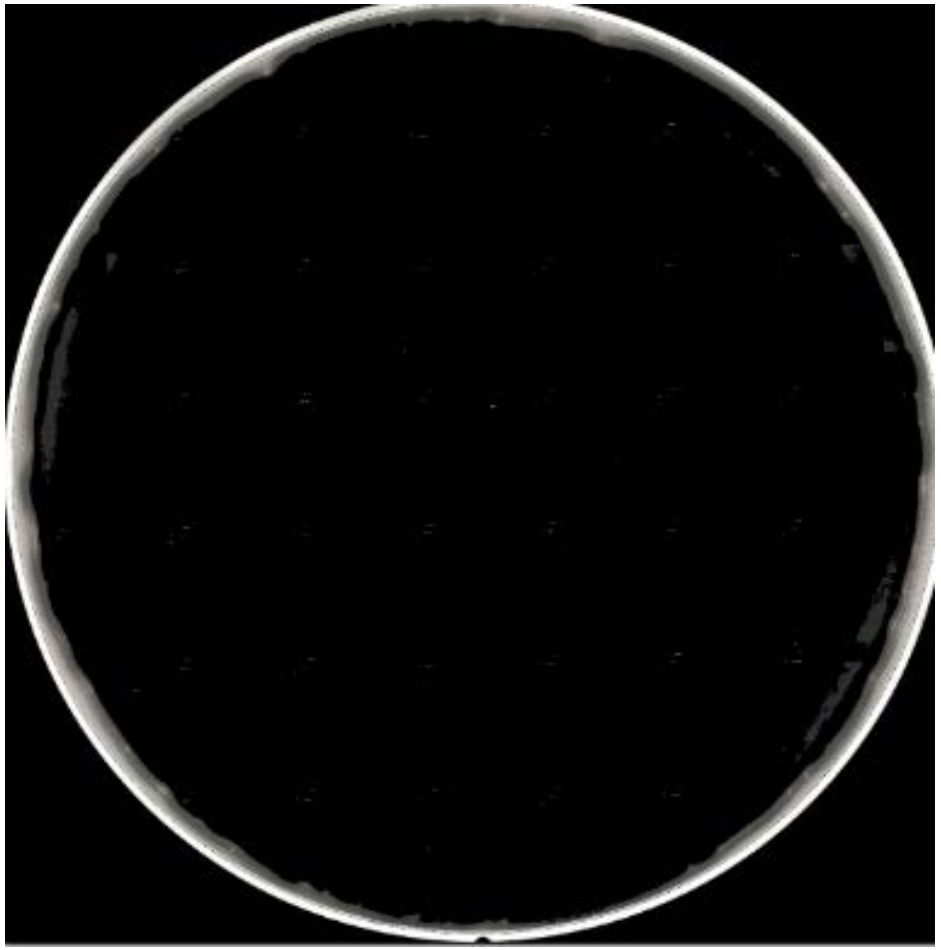


Possible Cracks in the LTO oxide

UHDI ETV – LTO vs. HTO SAM Results



Low Temperature Oxide SAM after final bond anneal

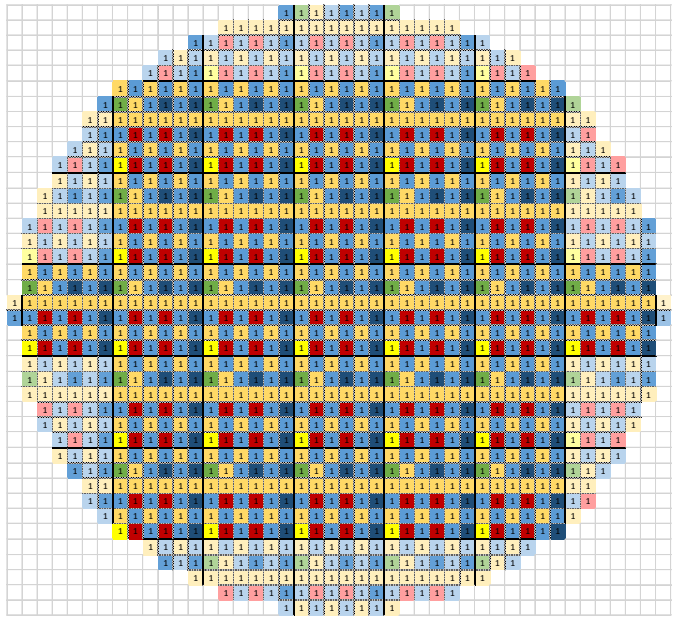


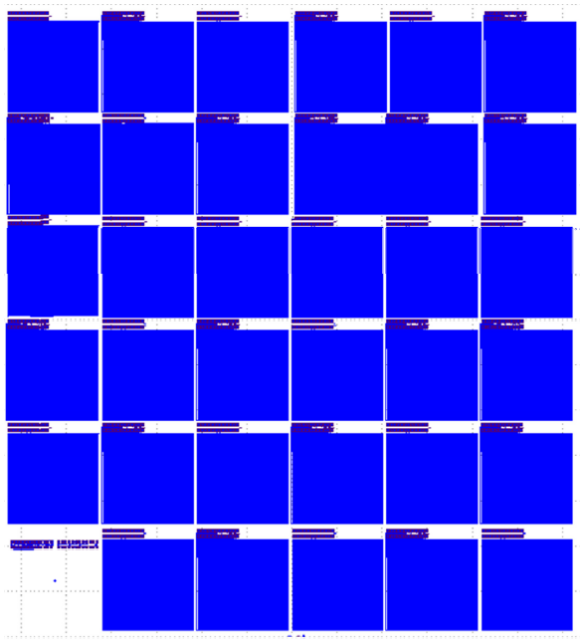
High Temperature Oxide SAM after final bond anneal

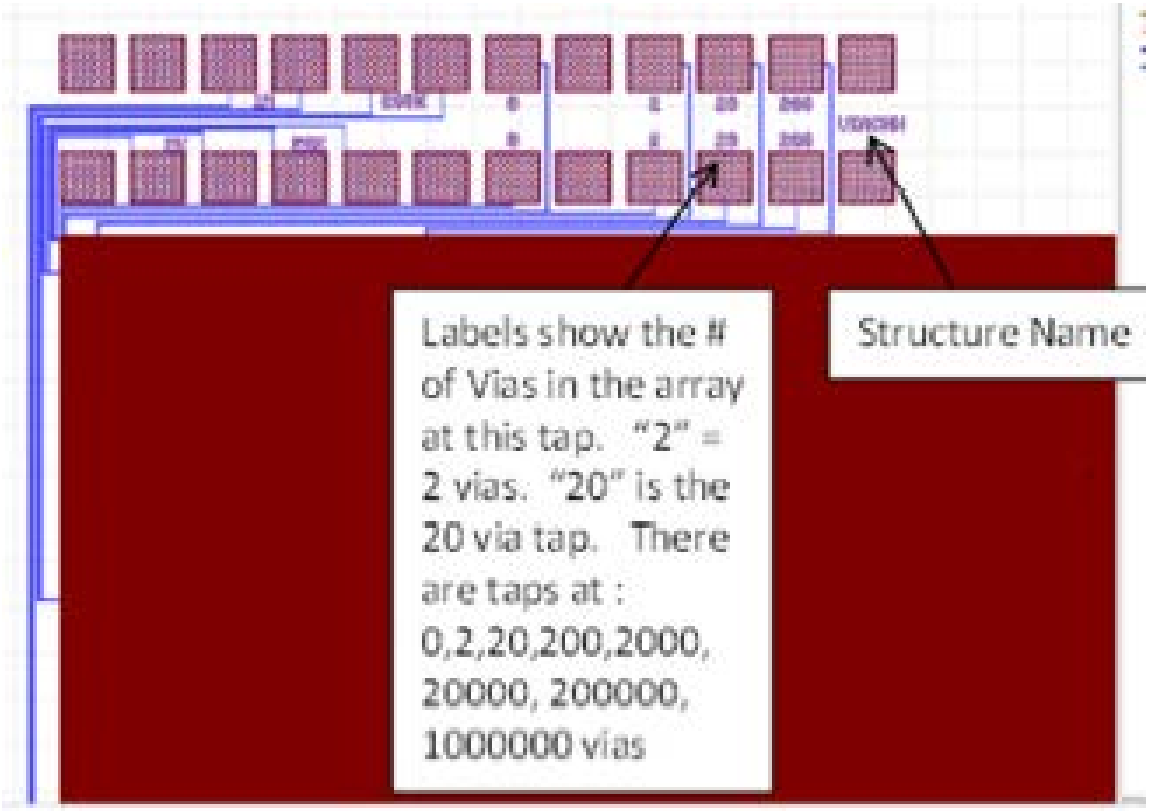
Scanning Acoustic Microscopy images indicate better bonding results for the high temperature oxide process

High temperature oxide process is still compatible with FusedSi substrates

UHDI ETV HTO – 1M, 4-point Test Overview





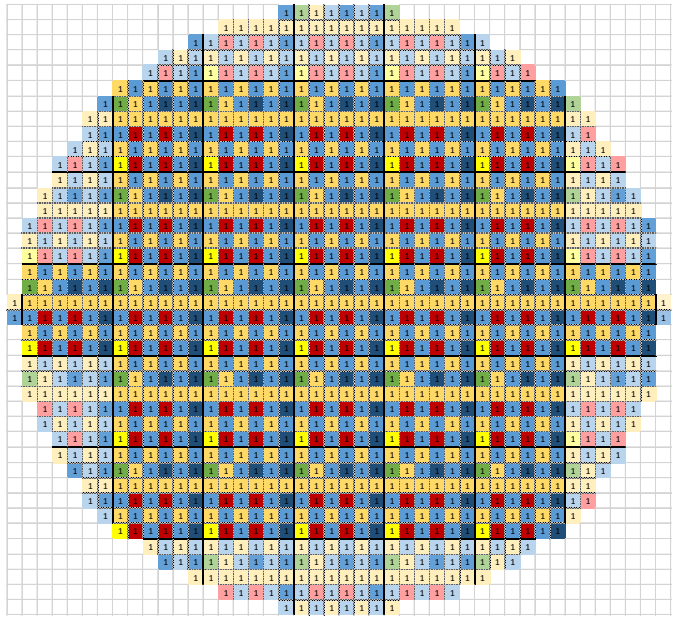


36 Cells per Die

- 13 standard 1M DBI via chains
  - taps @ 2,20,200,2k,20k,200k,1M
- 4 misaligned DBI via chains
  - -0.5, -0.25, +0.25, +0.5 µm
- 13 standard combs
- 4 misaligned combs
- 1 Serpentine Cell w/6 serpentines
  - M1/M2, 1/1.2/1.4 µm
- 1 EM Utility Cell

- 4-point test: 2 current carrying (mA), 2 voltage (V) sensing pads
- Individual mean via resistance ~80 milli-ohms

UHDI ETV HTO – 1M, 4-point Test Results

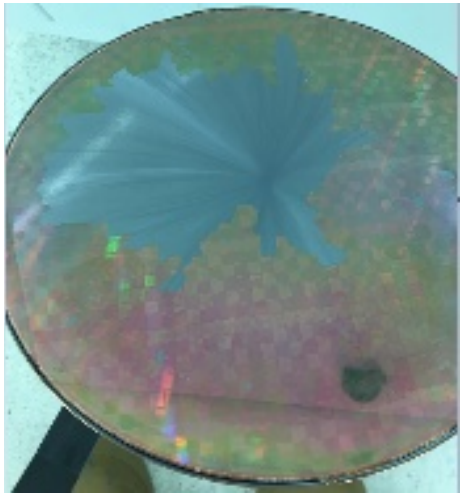


36 Cells per Die
- 13 standard 1M DBI via chains
  - taps @ 2,20,200,2k,20k,200k,1M
- 4 misaligned DBI via chains
  - -0.5, -0.25, +0.25, +0.5 µm
- 13 standard combs
- 4 misaligned combs
- 1 Serpentine Cell w/6 serpentines
  - M1/M2, 1/1.2/1.4 µm
- 1 EM Utility Cell

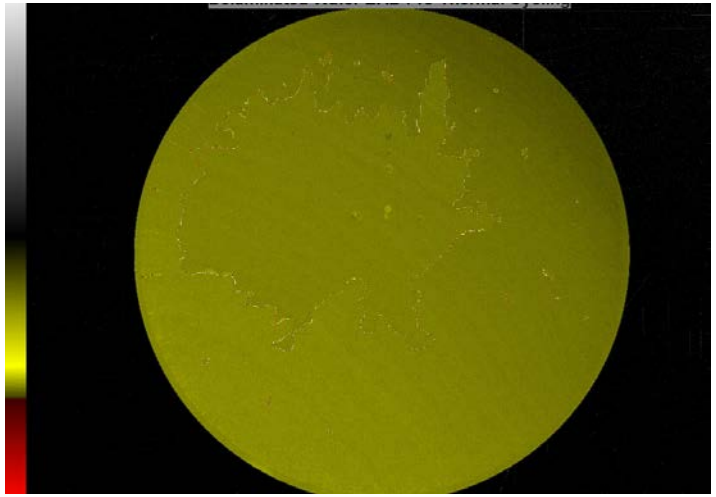
	W12	W11	W10	W9	W7	W5
V1M	15.1%	86.9%	3.6%	2.0%	2.0%	1.6%
V200K	62.5%	95.7%	44.6%	44.6%	42.9%	39.8%
V20K	92.9%	98.0%	88.5%	88.5%	88.9%	87.7%
V2000	96.4%	97.5%	98.6%	98.6%	95.1%	94.5%
V0200	98.8%	97.5%	98.6%	98.6%	97.4%	97.4%
V0020	99.2%	97.8%	98.6%	98.6%	97.5%	98.1%
V0002	99.2%	97.8%	98.6%	98.6%	97.5%	98.1%

- High Yield on 1M chains on wafer 11, ~87%!
  - Impacted by via lithography defects, CMP tiling bridging
- Project yield impacted by oxide deposition, metal line density

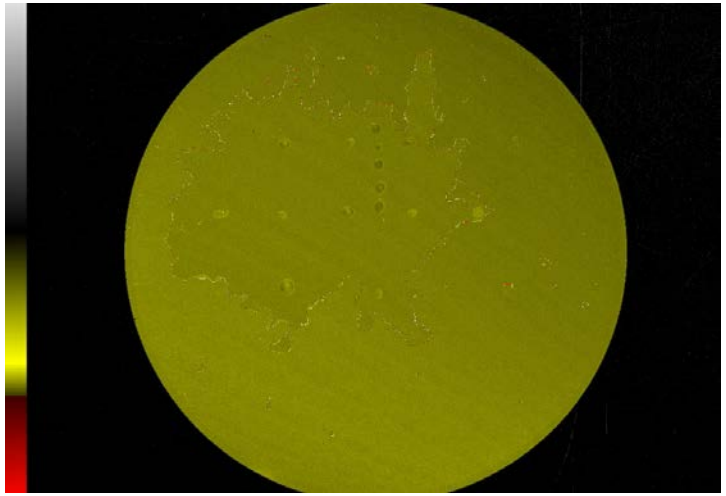
UHDI ETV HTO – Thermal Cycling Overview



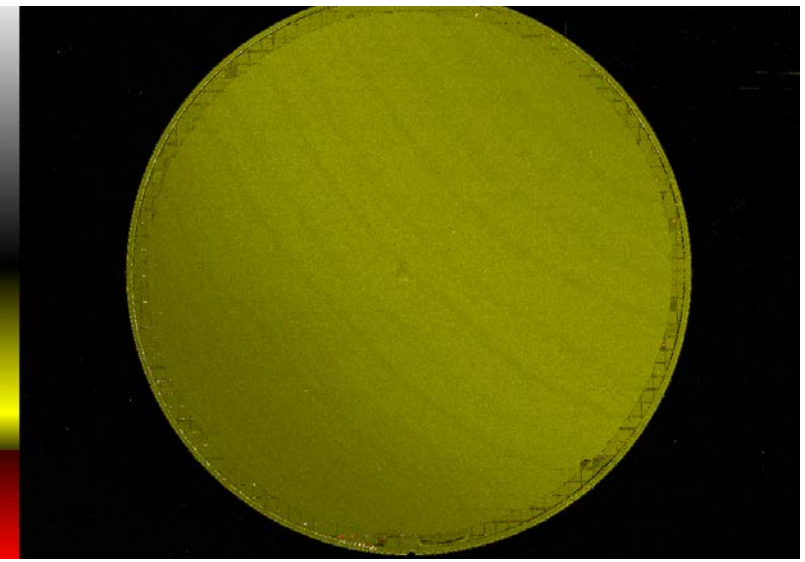
De-bonded LTO Send Ahead



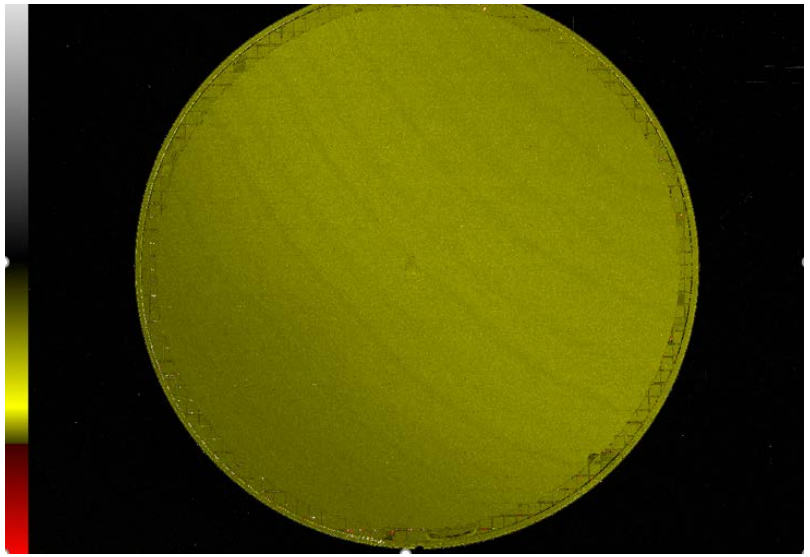
De-bonded LTO Pre Thermal Cycle



De-bonded LTO Post Thermal Cycle



Wafer 7 HTO Pre Thermal Cycle

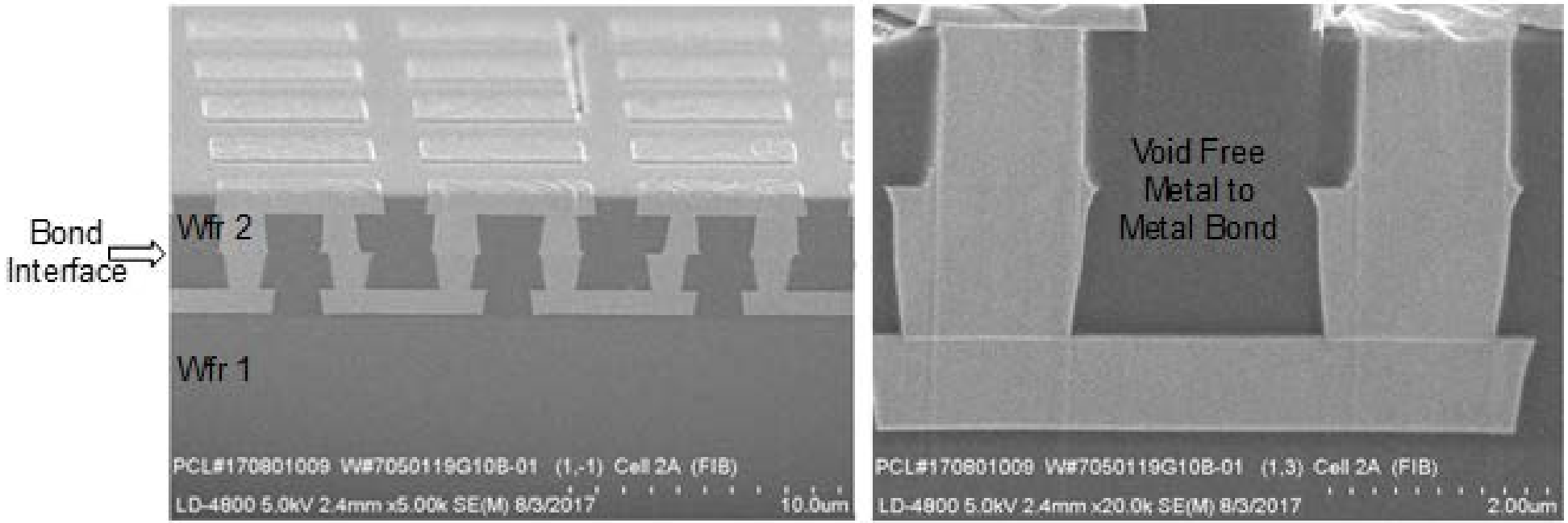


Wafer 7 HTO Post Thermal Cycle

- Thermal Cycle
  - -65C to 200C
  - 20mins, 6mins each zone
  - 10, 50, 100 cycles
- LTO send ahead showed additional de-bonding, as expected
- Initial HTO showed no effects and electrical data stayed consistent

UHDI ETV HTO – Summary

The first results have demonstrated bond yields (defined as 1M electrically connected I/O per die) of 87% across the entire wafer.



FIB cross-section images of the bonding interface after the top silicon has been etched away revealing the daisy chain circuitry and a void free bond across the dielectric and metal interfaces

Overview

NEOCITY and BRIDG overview

- Fab site and facility
- Equipment
- Roadmap

Advanced System Integration Program

- Ultra High Density Interposer Project

Next Steps

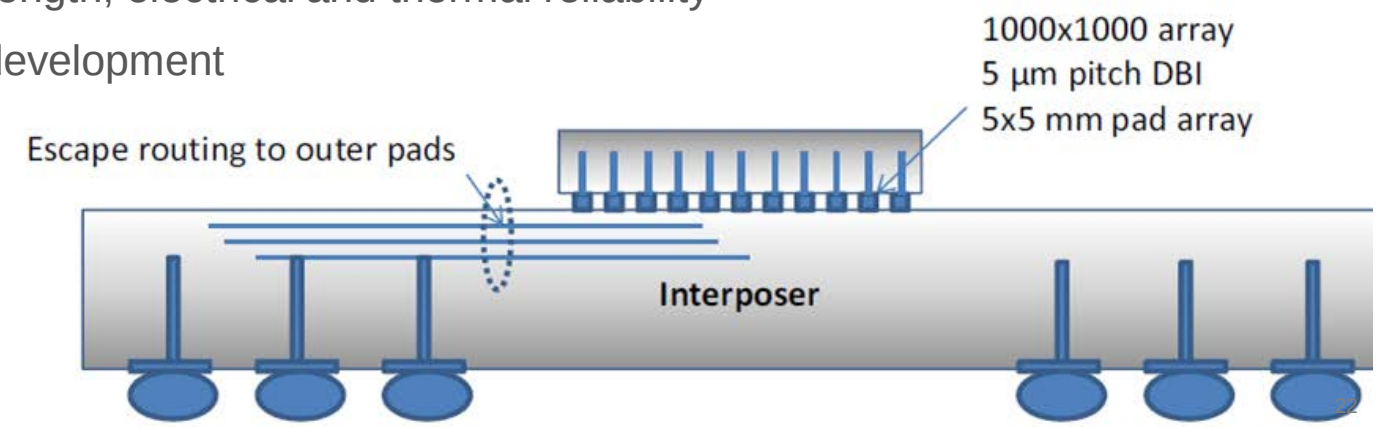
Next Steps

UHDI Multi-Layer Cu Routing

- Assessment of multi-layer routing/lithography schemes for connecting to Cu interconnect with a 4 um pitch and fanning out to a 40 – 120 um pitch
- Through substrate via fabrication feasibility to include via structures capped with at least one layer of dual damascene Cu interconnect for reliability studies
- Finite element modeling of Through Substrate Vias (TSV or TGV) to determine thermo-mechanical and electrical fidelity
- Integrated system deployment

UHDI Bonding and Electrical Characterization

- New mask-set design focused on 1M I/O test structure with complete DRC after pattern fill
- Fabricate 200mm bonding test wafers for process development at BRIDG and at suppliers, including silicon and fused silica
- Bond integrity testing to improve quality, including bond strength, electrical and thermal reliability
- Aggressive shrink of 1M I/O test structure to drive further development



Thank you!!!

Join Us!!!

UNIVERSITY OF
CENTRAL FLORIDA

To Learn about our Membership and Industry-friendly Partnerships, contact

BRIDG
200 NeoCity Way
NeoCity, FL 34744
(407) 742-4253

Dr. John Allgair
jallgair@gobridg.com

GoBRIDG.com